



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Docket No: Q63945

Hiroki KOIKE

Appln. No.: 09/824,751

Group Art Unit: 2818

Confirmation No.: 9722

Examiner: Unknown

Filed: April 04, 2001

For: SEMICONDUCTOR MEMORY DEVICE AND TESTING SYSTEM AND TESTING

METHOD

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §§ 1.97 and 1.98

Commissioner for Patents Washington, D.C. 20231

Sir:

APR 10 2003

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the document which is listed on the attached PTO/SB/08 A & B (modified) form and/or listed herein and which the Examiner may deem material to patentability of the claims of the above-identified application.

- 1. Japanese Unexamined Patent Publication No. 10-233100, published September 2, 1998. (This reference was previously submitted to the U.S. PTO with an Information Disclosure Statement dated April 4, 2001 so therefore a copy is not being enclosed herewith.)
- 2. Japanese Unexamined Patent Publication No. 09-097496, published April 8, 1997 (Abstract only)

One copy of Reference 2 submitted herewith.

The present Information Disclosure Statement is being filed: (1) No later than three months from the application's filing date for an application other than a continued prosecution application (CPA) under §1.53(d); (2) Before the mailing date of the first Office Action on the

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Information Disclosure Statement

merits (whichever is later); or (3) Before the mailing date of the first Office Action after filing a

request for continued examination (RCE) under §1.114, and therefore, no Statement under

37 C.F.R. § 1.97(e) or fee under 37 C.F.R. § 1.17(p) is required.

In compliance with the concise explanation requirement under 37 C.F.R. § 1.98(a)(3) for

foreign language documents, Applicant encloses herewith a copy of a Japanese translation of a

Korean Office Action dated January 27, 2003 as well as an English translation of the pertinent

portions of the Japanese translation. The Office Action cites such documents and indicates the

degree of relevance found by the foreign patent office.

The submission of the listed document is not intended as an admission that any such

document constitutes prior art against the claims of the present application. Applicant does not

waive any right to take any action that would be appropriate to antedate or otherwise remove any

listed document as a competent reference against the claims of the present application.

Respectfully submitted,

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WASHINGTON OFFICE

Date: APR 0 9 2003

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Reason 2

The invention described in the Scope of Patent Claims of this application could have been easily invented by a person having ordinary knowledge in the technical field of the invention prior to the filing of this application, and thus cannot be patented as per the stipulations of Article 29, Section 2 of the Patent Law.

Note

The present application relates to a semiconductor memory device, a test system and a test method capable of precisely determining the analogue data signal potential read on the bitline from a memory cell (bitline read potential).

The inventions described in Claims 1 and 2, when compared to the technology described in Japanese Unexamined Patent Application Publication H10-233100 (98.9.2) for a semiconductor memory device and inspection method thereof, comprising a cell [illegible], bitline and wordline potential raising means, bit potential detection means and the like, and compared to the standard potential generation technology described in Japanese Unexamined Patent Application Publication H9-97496 (97.4.8) for a ferroelectric memory device, comprise a partial difference in constitution, but this does not go beyond what could be achieved in this technical field by a simple design modification.

(Attachments)

Attachment 1 Japanese Unexamined Patent Application Publication H10-233100 (98.9.2)

Attachment 2 Japanese Unexamined Patent Application Publication H9-97496 (97.4.8) END